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NIPPON PRECISION CIRCUITS INC.

SM5009 series

Crystal Oscillator Module ICs

OVERVIEW

The SM5009 series are crystal oscillator module ICs that incorporate low crystal current type oscillating circuit to limit oscillator-stage current, so that they can reduce crystal current lower than the existing products. Since the oscillating circuit has oscillator capacitors with excellent frequency response and feedback resistor built-in, just connecting crystal realizes stable fundamental oscillation responding up to 40MHz. The SM5009 series are ideal for SMD type crystal oscillator using a strip-shaped crystal blank.

FEATURES

- Low crystal current oscillator
- Up to 40MHz operating frequency range (fundamental oscillation)
- Operating supply voltage range
  - 3V operation: 2.7 to 3.6V
  - 5V operation: 4.5 to 5.5V
- –40 to 85°C operating temperature range
- Oscillation capacitors C_G, C_D built-in
- Inverter amplifier feedback resistor built-in
- Standby function
  - Oscillator stops (AL series), high impedance in standby mode
- Low standby current
  - Power-save pull-up resistor built-in (AL series)
- Frequency divider built-in (f_O, $f_O/2$, $f_O/4$, $f_O/8$, $f_O/16$, $f_O/32$ determined by internal connection)
- Output drive capability
  - AL×, AN×, AK×, CN×: 16mA (V_{DD} = 4.5V)
  - AH×: 4mA (V_{DD} = 4.5V)
- Output load: C_L = 50pF max.
- Output duty level
  - CMOS level (1/2 VDD): AL×, AN×, AH×, CN×
  - TTL level (1.4V): AK×
- Molybdenum-gate CMOS process
- 8-pin SOP (SM5009×××S)
- Chip form (CF5009×××)

SERIES CONFIGURATION

Version[1]	3V operation		5V operation		Output duty level	Output frequency	$\overline{INH}$ Input level	Standby mode	
	Recommended operating frequency range[2] [MHz]	Output load[3] (max) [pF]	Recommended operating frequency range[2] [MHz]	Output load[3] (max) [pF]				Oscillator stop function	Output state
CF5009AL1	Up to 40	50	Up to 40	50	CMOS	f_O	CMOS	Yes	Hi-Z
CF5009AL2						$f_O/2$			
CF5009AL3						$f_O/4$			
CF5009AL4						$f_O/8$			
CF5009AL5						$f_O/16$			
CF5009AL6						$f_O/32$			
CF5009AN1	Up to 40	30	Up to 40	50	CMOS	f_O	TTL	No	Hi-Z
CF5009AN2						$f_O/2$			
CF5009AN3					CMOS/TTL	$f_O/4$			
CF5009AN4						$f_O/8$			
CF5009AN5						$f_O/16$			
CF5009AN6						$f_O/32$			
CF5009CN1	Up to 30	15	Up to 30	50	CMOS	f_O	TTL	No	Hi-Z
CF5009CN2						$f_O/2$			
CF5009AK1	–	–	Up to 40	15	TTL	f_O	TTL	No	Hi-Z
CF5009AK2						$f_O/2$			
CF5009AH1	Up to 16	15	Up to 30	15	CMOS	f_O	TTL	No	Hi-Z
CF5009AH2						$f_O/2$			
CF5009AH3						$f_O/4$			
CF5009AH4						$f_O/8$			

1. Package devices (8-pin SOP) have designation SM5009×××S.
2. The recommended operating frequency is a yardstick value derived from the crystal used for NPC characteristics authentication. However, the oscillator frequency band is not guaranteed. Specifically, the characteristics can vary greatly due to crystal characteristics and mounting conditions, so the oscillation characteristics of components must be carefully evaluated.
3. Output load value is the maximum load capacitance that allows drive.

APPLICATIONS

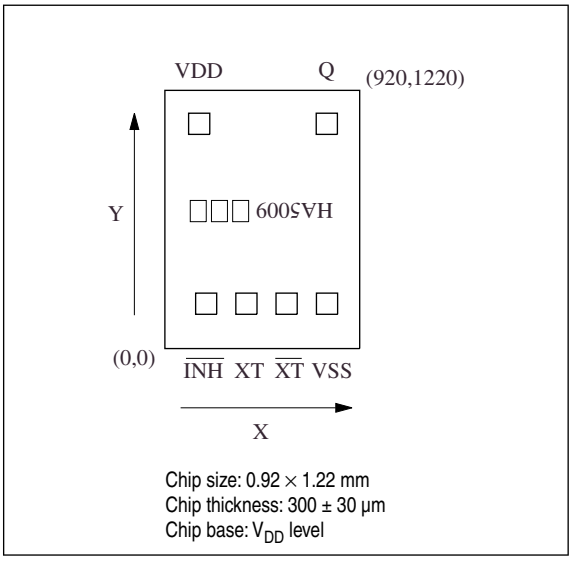
- SMD type crystal oscillator module

ORDERING INFORMATION

Device	Package
SM5009×××S	8-pin SOP
CF5009×××–1	Chip form

PAD LAYOUT

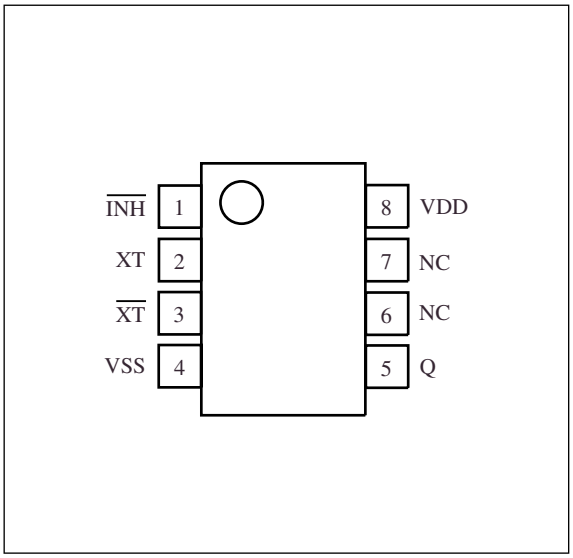
(Unit: µm)



Chip size: 0.92 × 1.22 mm
Chip thickness: 300 ± 30 µm
Chip base: V_{DD} level

PINOUT

(Top view)



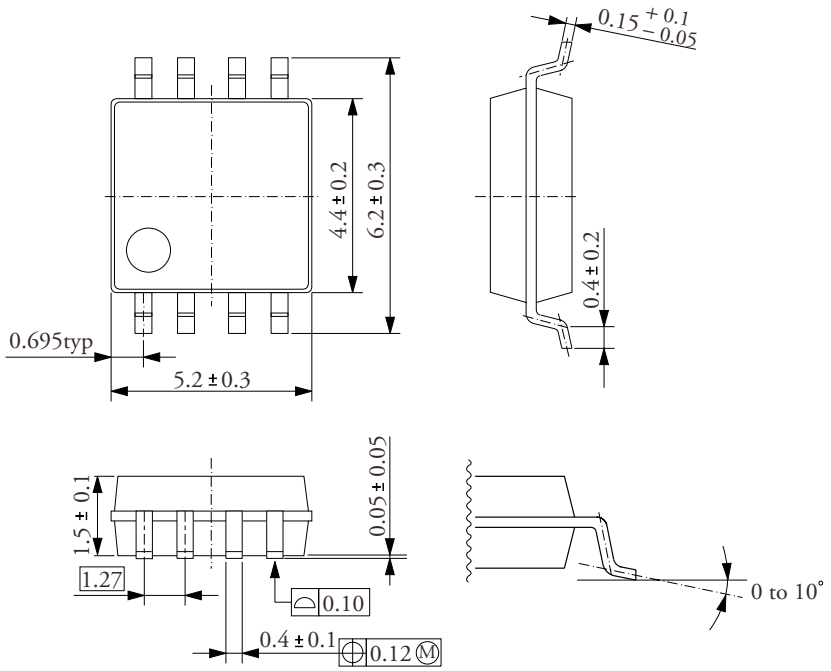
PIN DESCRIPTION and PAD DIMENSIONS

Number	Name	I/O	Description		Pad dimensions [µm]	
					X	Y
1	$\overline{INH}$	I	Output state control input. Standby mode when LOW, pull-up resistor built-in. In the case of the CF5009AL×, the oscillator stops and power-save pull-up resistor built in to reduce current consumption at standby mode.		195	212
2	XT	I	Amplifier input.	Crystal oscillator connection pins. Crystal oscillator connected between XT and $\overline{XT}$	385	212
3	$\overline{XT}$	O	Amplifier output.		575	212
4	VSS	–	Ground		766	212
5	Q	O	Output. Output frequency (f_O, $f_O/2$, $f_O/4$, $f_O/8$, $f_O/16$, $f_O/32$) determined by internal connection		765	1062
6	NC	–	No connection		–	–
7	NC	–	No connection		–	–
8	VDD	–	Supply voltage		162	1062

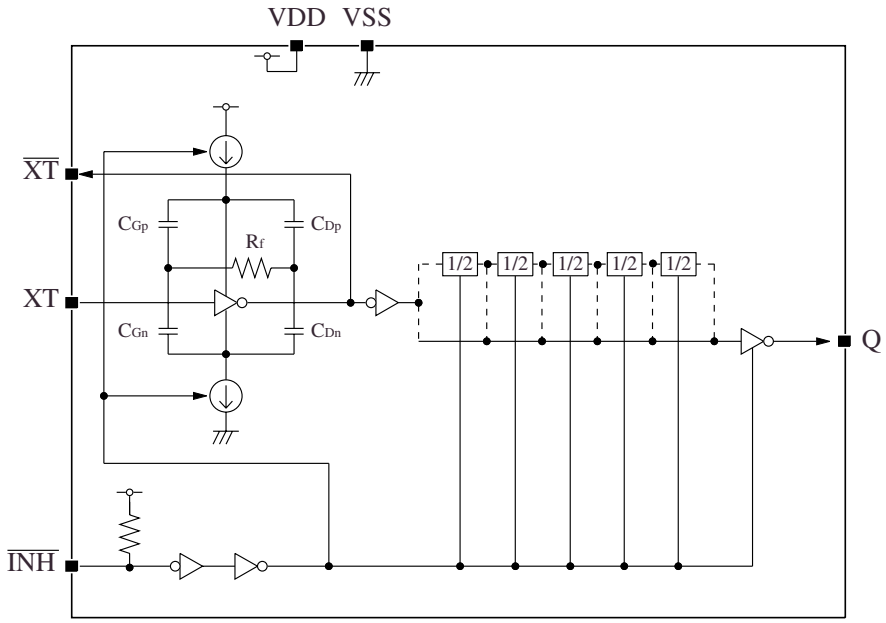
PACKAGE DIMENSIONS

(Unit: mm)

• 8-pin SOP



BLOCK DIAGRAM



Notes. The SM5009 series reduce crystal current by limiting driving current of oscillating-stage inverter and inhibiting oscillating amplitude. Depending on the characteristics of using crystal or the mounting condition, they may not oscillate normally. Please evaluate the oscillation start-up characteristics adequately with your actual device.

FUNCTIONAL DESCRIPTION

Standby Function

5009 AL× series

When $\overline{INH}$ goes LOW, the oscillator stops and the oscillator output on Q becomes high impedance.

5009AH×, AK×, AN×, CN× series

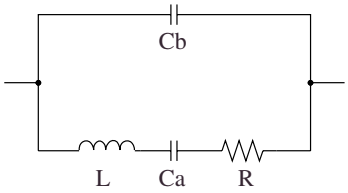
When $\overline{INH}$ goes LOW, the output on Q becomes high impedance, but internally the oscillator does not stop.

Version	$\overline{INH}$	Q	Oscillator
AL× series	HIGH (or open)	Any f_O , $f_O/2$, $f_O/4$, $f_O/8$, $f_O/16$ or $f_O/32$ output frequency	Normal operation
	LOW	High impedance	Stopped
AH×, AK×, AN×, CN× series	HIGH (or open)	Any f_O , $f_O/2$, $f_O/4$, $f_O/8$, $f_O/16$ or $f_O/32$ output frequency	Normal operation
	LOW	High impedance	Normal operation

Power-save Pull-up Resistance (AL× series only)

The $\overline{INH}$ pull-up resistance changes in response to the input level (HIGH or LOW). When $\overline{INH}$ goes LOW (standby state), the pull-up resistance becomes large to reduce the current consumption during standby.

Current consumption and Output waveform with NPC's standard crystal



f [MHz]	R [Ω]	L [mH]	Ca [fF]	Cb [pF]
30	17.2	4.36	6.46	2.26
40	16.8	2.90	5.47	2.08

SPECIFICATIONS

Absolute Maximum Ratings

V_{SS} = 0V unless otherwise noted.

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range	V_{DD}		–0.5 to +7.0	V
Input voltage range	V_{IN}		–0.5 to V_{DD} + 0.5	V
Output voltage range	V_{OUT}		–0.5 to V_{DD} + 0.5	V
Operating temperature range	T_{opr}		–40 to +85	°C
Storage temperature range	T_{stg}	Chip form	–65 to +150	°C
		8-pin SOP	–55 to +125	
Output current	I_{OUT}		25	mA
Power dissipation	P_D	8-pin SOP	500	mW

Recommended Operating Conditions

V_{SS} = 0V unless otherwise noted.

Parameter	Symbol	Version	Condition		Rating min	Rating typ	Rating max	Unit
Supply voltage	V_{DD}	AH×	f ≤ 30MHz		4.5	–	5.5	V
			f ≤ 16MHz		2.7	–	3.3	
		AK×	f ≤ 40MHz		4.5	–	5.5	V
		AN×	f ≤ 40MHz		2.7	–	5.5	V
		CN×	f ≤ 30MHz		2.7	–	5.5	V
		AL×	Chip form	f ≤ 40MHz	2.7	–	5.5	V
				f ≤ 30MHz	2.3	–	2.7	
				f ≤ 20MHz	2.25	–	2.75	
			8-pin SOP	f ≤ 40MHz	2.7	–	5.5	
				f ≤ 14.4MHz	2.4	–	2.7	
Input voltage	V_{IN}	All version			V_{SS}	–	V_{DD}	V
Operating temperature	T_{OPR}	AH×	f ≤ 30MHz, 4.5V ≤ V_{DD} ≤ 5.5V		– 40	–	+ 85	°C
			f ≤ 16MHz, 2.7V ≤ V_{DD} ≤ 3.6V		– 20	–	+ 80	
		AK×	f ≤ 30MHz		– 40	–	+ 85	°C
			30MHz < f ≤ 40MHz		– 20	–	+ 80	
		AN×	Chip form	f ≤ 40MHz, 2.7V ≤ V_{DD} < 4.5V	– 20	–	+ 80	°C
				f ≤ 40MHz, 4.5V ≤ V_{DD} ≤ 5.5V	– 40	–	+ 85	
			8-pin SOP	f ≤ 40MHz, 2.7V ≤ V_{DD} < 4.5V	– 20	–	+ 80	
				f ≤ 40MHz, 4.5V ≤ V_{DD} ≤ 5.5V	– 20	–	+ 80	
				f ≤ 30MHz, 4.5V ≤ V_{DD} ≤ 5.5V	– 40	–	+ 85	
		CN×	f ≤ 30MHz, 2.7V ≤ V_{DD} < 4.5V		– 10	–	+ 70	°C
			f ≤ 30MHz, 4.5V ≤ V_{DD} ≤ 5.5V		– 40	–	+ 85	
		AL×	Chip form	f ≤ 40MHz, 2.7V ≤ V_{DD} ≤ 5.5V	– 40	–	+ 85	°C
				f ≤ 30MHz, 2.3V ≤ V_{DD} ≤ 2.7V	– 20	–	+ 80	
				f ≤ 20MHz, 2.25V ≤ V_{DD} ≤ 2.75V	– 20	–	+ 80	
			8-pin SOP	f ≤ 40MHz, 2.7V ≤ V_{DD} ≤ 5.5V	– 20	–	+ 80	
				f ≤ 30MHz, 2.7V ≤ V_{DD} ≤ 5.5V	– 40	–	+ 85	
				f ≤ 14.4MHz, 2.4V ≤ V_{DD} ≤ 2.7V	– 20	–	+ 80	

Electrical Characteristics

5009AL× series

3V operation: V_{DD} = 2.7 to 3.3V, V_{SS} = 0V, Ta = –40 to 85°C unless otherwise noted.

Parameter	Symbol	Condition		Rating			Unit
				min	typ	max	
HIGH-level output voltage	V_{OH}	Q: Measurement cct 1, I_{OH} = 8mA		2.2	–	–	V
LOW-level output voltage	V_{OL}	Q: Measurement cct 1, I_{OL} = 8mA		–	–	0.4	V
HIGH-level input voltage	V_{IH}	$\overline{INH}$		0.7V_{DD}	–	–	V
LOW-level input voltage	V_{IL}	$\overline{INH}$		–	–	0.3V_{DD}	V
Output leakage current	I_Z	Q: Measurement cct 2, $\overline{INH}$ = LOW, V_{OH} = V_{DD}		–	–	10	µA
		Q: Measurement cct 2, $\overline{INH}$ = LOW, V_{OL} = V_{SS}		–	–	10	
Current consumption	I_{DD}	$\overline{INH}$ = open, Measurement cct 3, load cct 2, C_L = 15pF, 40MHz crystal oscillator	CF5009AL1	–	8	17	mA
			CF5009AL2	–	5	11	
			CF5009AL3	–	4	9	
			CF5009AL4	–	3	7	
			CF5009AL5	–	3	6	
			CF5009AL6	–	2	5	
		$\overline{INH}$ = open, Measurement cct 3, load cct 2, C_L = 15pF, 40MHz crystal oscillator, Ta = –20 to +80°C	SM5009AL1S	–	8	17	
			SM5009AL2S	–	5	11	
			SM5009AL3S	–	4	9	
			SM5009AL4S	–	3	7	
			SM5009AL5S	–	3	6	
			SM5009AL6S	–	2	5	
Standby current	I_{ST}	$\overline{INH}$ = V_{SS}, Measurement cct 3		–	2	5	µA
$\overline{INH}$ pull-up resistance	R_{UP1}	Measurement cct 4, V_{DD} = 3V, $\overline{INH}$ = V_{SS}		0.6	–	12	MΩ
	R_{UP2}	Measurement cct 4, V_{DD} = 3V, $\overline{INH}$ = 2.1V		40	–	200	kΩ
Negative resistance	$-R_L$	V_{DD} = 3V, Ta = 25°C, 40MHz		–	–200	–	Ω
Feedback resistance	R_f	Measurement cct 5		0.4	–	1.1	MΩ
Built-in capacitance	C_G	Design value. A monitor pattern on a wafer is tested.		5.58	6	6.42	pF
	C_D			9.3	10	10.7	pF

5V operation: V_{DD} = 4.5 to 5.5V, V_{SS} = 0V, Ta = –40 to 85°C unless otherwise noted.

Parameter	Symbol	Condition		Rating min	Rating typ	Rating max	Unit
HIGH-level output voltage	V_{OH}	Q: Measurement cct 1, I_{OH} = 16mA		4.0	–	–	V
LOW-level output voltage	V_{OL}	Q: Measurement cct 1, I_{OL} = 16mA		–	–	0.4	V
HIGH-level input voltage	V_{IH}	$\overline{INH}$		$0.7V_{DD}$	–	–	V
LOW-level input voltage	V_{IL}	$\overline{INH}$		–	–	$0.3V_{DD}$	V
Output leakage current	I_Z	Q: Measurement cct 2, $\overline{INH}$ = LOW, $V_{OH} = V_{DD}$		–	–	10	µA
		Q: Measurement cct 2, $\overline{INH}$ = LOW, $V_{OL} = V_{SS}$		–	–	10	
Current consumption	I_{DD}	$\overline{INH}$ = open, Measurement cct 3, load cct 2, C_L = 15pF, 40MHz crystal oscillator	CF5009AL1	–	12	26	mA
			CF5009AL2	–	8	17	
			CF5009AL3	–	6	13	
			CF5009AL4	–	5	11	
			CF5009AL5	–	5	10	
			CF5009AL6	–	4	9	
		$\overline{INH}$ = open, Measurement cct 3, load cct 2, C_L = 15pF, 40MHz crystal oscillator, Ta = –20 to +80°C	SM5009AL1S	–	12	26	
			SM5009AL2S	–	8	17	
			SM5009AL3S	–	6	13	
			SM5009AL4S	–	5	11	
			SM5009AL5S	–	5	10	
			SM5009AL6S	–	4	9	
Standby current	I_{ST}	$\overline{INH} = V_{SS}$, Measurement cct 3		–	6	15	µA
$\overline{INH}$ pull-up resistance	R_{UP1}	Measurement cct 4, V_{DD} = 5V, $\overline{INH} = V_{SS}$		0.3	–	6	MΩ
	R_{UP2}	Measurement cct 4, V_{DD} = 5V, $\overline{INH}$ = 3.5V		40	–	200	kΩ
Negative resistance	$-R_L$	V_{DD} = 5V, Ta = 25°C, 40MHz		–	–400	–	Ω
Feedback resistance	R_f	Measurement cct 5		0.4	–	1.1	MΩ
Built-in capacitance	C_G	Design value. A monitor pattern on a wafer is tested.		5.58	6	6.42	pF
	C_D			9.3	10	10.7	pF

5009AN×/CN× series

3V operation: V_{DD} = 2.7 to 3.3V, V_{SS} = 0V, Ta = −20 to 80°C unless otherwise noted.

Parameter	Symbol	Condition		Rating min	Rating typ	Rating max	Unit
HIGH-level output voltage	V_{OH}	Q: Measurement cct 1, I_{OH} = 8mA	SM5009AN1S, CF5009AN1 SM5009AN2S, CF5009AN2	2.2	–	–	V
			SM5009AN3S, CF5009AN3 SM5009AN4S, CF5009AN4 SM5009AN5S, CF5009AN5 SM5009AN6S, CF5009AN6 SM5009CN1S, CF5009CN1 SM5009CN2S, CF5009CN2	2.1	–	–	
LOW-level output voltage	V_{OL}	Q: Measurement cct 1, I_{OL} = 8mA		–	–	0.4	V
HIGH-level input voltage	V_{IH}	$\overline{INH}$		2.0	–	–	V
LOW-level input voltage	V_{IL}	$\overline{INH}$		–	–	0.3	V
Output leakage current	I_Z	Q: Measurement cct 2, $\overline{INH}$ = LOW, $V_{OH} = V_{DD}$		–	–	10	µA
		Q: Measurement cct 2, $\overline{INH}$ = LOW, $V_{OL} = V_{SS}$		–	–	10	
Current consumption	I_{DD}	$\overline{INH}$ = open, Measurement cct 3, load cct 2, C_L = 15pF, 40MHz crystal oscillator	SM5009AN1S, CF5009AN1	–	8	17	mA
			SM5009AN2S, CF5009AN2	–	5	11	
			SM5009AN3S, CF5009AN3	–	4	9	
			SM5009AN4S, CF5009AN4	–	3	7	
			SM5009AN5S, CF5009AN5	–	3	6	
			SM5009AN6S, CF5009AN6	–	2	5	
		$\overline{INH}$ = open, Measurement cct 3, load cct 2, C_L = 15pF, 30MHz crystal oscillator, Ta = −10 to +70°C	SM5009CN1S, CF5009CN1	–	7	15	
			SM5009CN2S, CF5009CN2	–	4	9	
$\overline{INH}$ pull-up resistance	R_{UP}	Measurement cct 4, V_{DD} = 3V, $\overline{INH} = V_{SS}$		40	–	200	kΩ
Negative resistance	$-R_L$	V_{DD} = 3V, Ta = 25°C, 40MHz		–	−100	–	Ω
Feedback resistance	R_f	Measurement cct 5		0.4	–	1.1	MΩ
Built-in capacitance	C_G	Design value. A monitor pattern on a wafer is tested.		5.58	6	6.42	pF
	C_D			9.3	10	10.7	pF

5V operation: V_{DD} = 4.5 to 5.5V, V_{SS} = 0V, Ta = –40 to 85°C unless otherwise noted.

Parameter	Symbol	Condition		Rating min	Rating typ	Rating max	Unit
HIGH-level output voltage	V_{OH}	Q: Measurement cct 1, I_{OH} = 16mA	SM5009AN1S, CF5009AN1 SM5009AN2S, CF5009AN2	4.0	–	–	V
			SM5009AN3S, CF5009AN3 SM5009AN4S, CF5009AN4 SM5009AN5S, CF5009AN5 SM5009AN6S, CF5009AN6 SM5009CN1S, CF5009CN1 SM5009CN2S, CF5009CN2	3.9	–	–	
LOW-level output voltage	V_{OL}	Q: Measurement cct 1, I_{OL} = 16mA		–	–	0.4	V
HIGH-level input voltage	V_{IH}	$\overline{INH}$		2.0	–	–	V
LOW-level input voltage	V_{IL}	$\overline{INH}$		–	–	0.8	V
Output leakage current	I_Z	Q: Measurement cct 2, $\overline{INH}$ = LOW, $V_{OH} = V_{DD}$		–	–	10	µA
		Q: Measurement cct 2, $\overline{INH}$ = LOW, $V_{OL} = V_{SS}$		–	–	10	
Current consumption	I_{DD}	$\overline{INH}$ = open, Measurement cct 3, load cct 2, C_L = 15pF, 40MHz crystal oscillator	CF5009AN1	–	12	26	mA
			CF5009AN2	–	8	17	
			CF5009AN3	–	6	13	
			CF5009AN4	–	5	11	
			CF5009AN5	–	5	10	
			CF5009AN6	–	4	9	
		$\overline{INH}$ = open, Measurement cct 3, load cct 2, C_L = 15pF, 40MHz crystal oscillator, Ta = –20 to +80°C	SM5009AN1S	–	12	26	
			SM5009AN2S	–	8	17	
			SM5009AN3S	–	6	13	
			SM5009AN4S	–	5	11	
			SM5009AN5S	–	5	10	
			SM5009AN6S	–	4	9	
		$\overline{INH}$ = open, Measurement cct 3, load cct 2, C_L = 15pF, 30MHz crystal oscillator	SM5009CN1S, CF5009CN1	–	10	22	
			SM5009CN2S, CF5009CN2	–	7	15	
$\overline{INH}$ pull-up resistance	R_{UP}	Measurement cct 4, V_{DD} = 5V, $\overline{INH} = V_{SS}$		40	–	200	kΩ
Negative resistance	$–R_L$	V_{DD} = 5V, Ta = 25°C, 40MHz		–	–210	–	Ω
Feedback resistance	R_f	Measurement cct 5		0.4	–	1.1	MΩ
Built-in capacitance	C_G	Design value. A monitor pattern on a wafer is tested.		5.58	6	6.42	pF
	C_D			9.3	10	10.7	pF

5009AK× series

V_{DD} = 4.5 to 5.5V, V_{SS} = 0V, Ta = –40 to 85°C unless otherwise noted.

Parameter	Symbol	Condition		Rating min	Rating typ	Rating max	Unit
HIGH-level output voltage	V_{OH}	Q: Measurement cct 1, I_{OH} = 16mA		4.0	–	–	V
LOW-level output voltage	V_{OL}	Q: Measurement cct 1, I_{OL} = 16mA		–	–	0.4	V
HIGH-level input voltage	V_{IH}	$\overline{INH}$		2.0	–	–	V
LOW-level input voltage	V_{IL}	$\overline{INH}$		–	–	0.8	V
Output leakage current	I_Z	Q: Measurement cct 2, $\overline{INH}$ = LOW, $V_{OH} = V_{DD}$		–	–	10	µA
		Q: Measurement cct 2, $\overline{INH}$ = LOW, $V_{OL} = V_{SS}$		–	–	10	
Current consumption	I_{DD}	$\overline{INH}$ = open, Measurement cct 3, load cct 1, C_L = 15pF, 40MHz crystal oscillator, Ta = –20 to +80°C	SM5009AK1S	–	12	26	mA
			CF5009AK1	–	12	26	
			SM5009AK2S	–	8	17	
			CF5009AK2	–	8	17	
$\overline{INH}$ pull-up resistance	R_{UP}	Measurement cct 4, V_{DD} = 5V, $\overline{INH} = V_{SS}$		40	–	200	kΩ
Negative resistance	$-R_L$	V_{DD} = 5V, Ta = 25°C, 40MHz		–	–210	–	Ω
Feedback resistance	R_f	Measurement cct 5		0.4	–	1.1	MΩ
Built-in capacitance	C_G	Design value. A monitor pattern on a wafer is tested.		5.58	6	6.42	pF
	C_D			9.3	10	10.7	pF

5009AH× series

3V operation: V_{DD} = 2.7 to 3.3V, V_{SS} = 0V, Ta = –20 to 80°C unless otherwise noted.

Parameter	Symbol	Condition		Rating min	Rating typ	Rating max	Unit
HIGH-level output voltage	V_{OH}	Q: Measurement cct 1, I_{OH} = 2mA		2.2	–	–	V
LOW-level output voltage	V_{OL}	Q: Measurement cct 1, I_{OL} = 2mA		–	–	0.4	V
HIGH-level input voltage	V_{IH}	$\overline{INH}$		2.0	–	–	V
LOW-level input voltage	V_{IL}	$\overline{INH}$		–	–	0.3	V
Output leakage current	I_Z	Q: Measurement cct 2, $\overline{INH}$ = LOW, V_{OH} = V_{DD}		–	–	10	µA
		Q: Measurement cct 2, $\overline{INH}$ = LOW, V_{OL} = V_{SS}		–	–	10	
Current consumption	I_{DD}	$\overline{INH}$ = open, Measurement cct 3, load cct 2, C_L = 15pF, 16MHz crystal oscillator	SM5009AH1S CF5009AH1	–	4.5	10	mA
			SM5009AH2S CF5009AH2	–	3	7	
			SM5009AH3S CF5009AH3 SM5009AH4S CF5009AH4	–	1.5	3.5	
$\overline{INH}$ pull-up resistance	R_{UP}	Measurement cct 4, V_{DD} = 3V, $\overline{INH}$ = V_{SS}		40	–	200	kΩ
Negative resistance	$-R_L$	V_{DD} = 3V, Ta = 25°C, 16MHz		–	–450	–	Ω
Feedback resistance	R_f	Measurement cct 5		0.4	–	1.1	MΩ
Built-in capacitance	C_G	Design value. A monitor pattern on a wafer is tested.		5.58	6	6.42	pF
	C_D			9.3	10	10.7	pF

5V operation: V_{DD} = 4.5 to 5.5V, V_{SS} = 0V, Ta = –40 to 85°C unless otherwise noted.

Parameter	Symbol	Condition		Rating min	Rating typ	Rating max	Unit
HIGH-level output voltage	V_{OH}	Q: Measurement cct 1, I_{OH} = 4mA		4.0	–	–	V
LOW-level output voltage	V_{OL}	Q: Measurement cct 1, I_{OL} = 4mA		–	–	0.4	V
HIGH-level input voltage	V_{IH}	$\overline{INH}$		2.0	–	–	V
LOW-level input voltage	V_{IL}	$\overline{INH}$		–	–	0.8	V
Output leakage current	I_Z	Q: Measurement cct 2, $\overline{INH}$ = LOW, V_{OH} = V_{DD}		–	–	10	µA
		Q: Measurement cct 2, $\overline{INH}$ = LOW, V_{OL} = V_{SS}		–	–	10	
Current consumption	I_{DD}	$\overline{INH}$ = open, Measurement cct 3, load cct 2, C_L = 15pF, 30MHz crystal oscillator	SM5009AH1S CF5009AH1	–	9	20	mA
			SM5009AH2S CF5009AH2	–	6	13	
			SM5009AH3S CF5009AH3 SM5009AH4S CF5009AH4	–	4	9	
$\overline{INH}$ pull-up resistance	R_{UP}	Measurement cct 4, V_{DD} = 5V, $\overline{INH}$ = V_{SS}		40	–	200	kΩ
Negative resistance	$-R_L$	V_{DD} = 5V, Ta = 25°C, 30MHz		–	–340	–	Ω
Feedback resistance	R_f	Measurement cct 5		0.4	–	1.1	MΩ
Built-in capacitance	C_G	Design value. A monitor pattern on a wafer is tested.		5.58	6	6.42	pF
	C_D			9.3	10	10.7	pF

Switching Characteristics

5009AL× series

3V operation: V_{DD} = 2.7 to 3.3V, V_{SS} = 0V, Ta = –40 to 85°C unless otherwise noted.

Parameter	Symbol	Condition		Rating min	Rating typ	Rating max	Unit
Output rise time	t_{r1}	Measurement cct 3, load cct 2, 0.1V_{DD} to 0.9V_{DD} , C_L = 15pF		–	3.5	9	ns
		Measurement cct 3, load cct 2, 0.1V_{DD} to 0.9V_{DD} , V_{DD} = 2.3 to 2.7V, Ta = –20 to +80°C, C_L = 15pF		–	4	13	
	t_{r2}	Measurement cct 3, load cct 2, 0.1V_{DD} to 0.9V_{DD} , C_L = 30pF		–	5	12	
		Measurement cct 3, load cct 2, 0.1V_{DD} to 0.9V_{DD} , V_{DD} = 2.4 to 2.7V, Ta = –20 to +80°C, C_L = 30pF		–	5.5	16	
	t_{r3}	Measurement cct 3, load cct 2, 0.1V_{DD} to 0.9V_{DD} , V_{DD} = 3.0 to 3.6V, f ≤ 30MHz, C_L = 50pF		–	5	12	
		Measurement cct 3, load cct 2, 0.2V_{DD} to 0.8V_{DD} , V_{DD} = 3.0 to 3.6V, f ≤ 40MHz, C_L = 50pF		–	3.5	12	
Output fall time	t_{f1}	Measurement cct 3, load cct 2, 0.9V_{DD} to 0.1V_{DD} , C_L = 15pF		–	3.5	9	ns
		Measurement cct 3, load cct 2, 0.9V_{DD} to 0.1V_{DD} , V_{DD} = 2.3 to 2.7V, Ta = –20 to +80°C, C_L = 15pF		–	4	13	
	t_{f2}	Measurement cct 3, load cct 2, 0.9V_{DD} to 0.1V_{DD} , C_L = 30pF		–	5	12	
		Measurement cct 3, load cct 2, 0.9V_{DD} to 0.1V_{DD} , V_{DD} = 2.4 to 2.7V, Ta = –20 to +80°C, C_L = 30pF		–	5.5	16	
	t_{f3}	Measurement cct 3, load cct 2, 0.9V_{DD} to 0.1V_{DD} , V_{DD} = 3.0 to 3.6V, f ≤ 30MHz, C_L = 50pF		–	5	12	
		Measurement cct 3, load cct 2, 0.8V_{DD} to 0.2V_{DD} , V_{DD} = 3.0 to 3.6V, f ≤ 40MHz, C_L = 50pF		–	3.5	12	
Output duty cycle[1]	Duty1	Measurement cct 3, load cct 2, V_{DD} = 3V, f ≤ 40MHz, Ta = 25°C, C_L = 30pF		45	–	55	%
		Measurement cct 3, load cct 2, V_{DD} = 2.4V, f ≤ 14.4MHz, Ta = 25°C, C_L = 30pF		40	–	60	
		CF5009AL× only, Measurement cct 3, load cct 2, V_{DD} = 2.5V, f ≤ 30MHz, Ta = 25°C, C_L = 15pF		40	–	60	
	Duty2	CF5009AL× only, Measurement cct 3, load cct 2, V_{DD} = 3.3V, f ≤ 30MHz, Ta = 25°C, C_L = 50pF		45	–	55	
		CF5009AL× only, Measurement cct 3, load cct 2, V_{DD} = 3.3V, f ≤ 40MHz, Ta = 25°C, C_L = 50pF		40	–	60	
Output disable delay time[2]	t_{PLZ}	Measurement cct 6, load cct 2, V_{DD} = 3V, Ta = 25°C, C_L ≤ 15pF		–	–	100	ns
Output enable delay time[2]	t_{PZL}			–	–	100	ns
Maximum operating frequency	f_{max}	Measurement cct 3	CF5009AL×	40	–	–	MHz
			SM5009AL×S	30	–	–	
		Measurement cct 3, Ta = –20 to +80°C	SM5009AL×S	40	–	–	
		Measurement cct 3, Ta = –20 to +80°C	V_{DD} = 2.4 to 2.7V, SM5009AL×S	14.4	–	–	
			V_{DD} = 2.3 to 2.7V, CF5009AL×	30	–	–	
			V_{DD} = 2.25 to 2.75V, CF5009AL×	20	–	–	

1. The duty cycle characteristic is checked the sample chips of each production lot.
2. Oscillator stop function is built-in. When $\overline{INH}$ goes LOW, normal output stops. When $\overline{INH}$ goes HIGH, normal output is not resumed until after the oscillator start-up time has elapsed.

5V operation: V_{DD} = 4.5 to 5.5V, V_{SS} = 0V, Ta = –40 to 85°C unless otherwise noted.

Parameter	Symbol	Condition		Rating min	Rating typ	Rating max	Unit
Output rise time	t_{r1}	Measurement cct 3, load cct 2, 0.1V_{DD} to 0.9V_{DD}	C_L = 15pF	–	2	4	ns
	t_{r2}		C_L = 30pF	–	3.5	7	
	t_{r3}		C_L = 50pF	–	4	8	
Output fall time	t_{f1}	Measurement cct 3, load cct 2, 0.9V_{DD} to 0.1V_{DD}	C_L = 15pF	–	2	4	ns
	t_{f2}		C_L = 30pF	–	3.5	7	
	t_{f3}		C_L = 50pF	–	4	8	
Output duty cycle[1]	Duty	Measurement cct 3, load cct 2, V_{DD} = 5V, Ta = 25°C, C_L = 50pF		45	–	55	%
Output disable delay time[2]	t_{PLZ}	Measurement cct 6, load cct 2, V_{DD} = 5V, Ta = 25°C, $C_L \leq$ 15pF		–	–	100	ns
Output enable delay time[2]	t_{PZL}			–	–	100	ns
Maximum operating frequency	f_{max}	Measurement cct 3	CF5009AL×	40	–	–	MHz
			SM5009AL×S	30	–	–	
		Measurement cct 3, Ta = –20 to +80°C	SM5009AL×S	40	–	–	

1. The duty cycle characteristic is checked the sample chips of each production lot.
2. Oscillator stop function is built-in. When $\overline{INH}$ goes LOW, normal output stops. When $\overline{INH}$ goes HIGH, normal output is not resumed until after the oscillator start-up time has elapsed.

5009AN×/CN× series

3V operation: V_{DD} = 2.7 to 3.3V, V_{SS} = 0V, Ta = −20 to 80°C unless otherwise noted.

Parameter	Symbol	Condition		Rating			Unit
				min	typ	max	
Output rise time	t_{r1}	Measurement cct 3, load cct 2, 0.1V_{DD} to 0.9V_{DD} ,C_L = 15pF	SM5009AN1S, CF5009AN1 SM5009AN2S, CF5009AN2	–	3.5	9	ns
			SM5009AN3S, CF5009AN3 SM5009AN4S, CF5009AN4 SM5009AN5S, CF5009AN5 SM5009AN6S, CF5009AN6 SM5009CN1S, CF5009CN1 SM5009CN2S, CF5009CN2	–	5	13	
	t_{r2}	Measurement cct 3, load cct 2, 0.1V_{DD} to 0.9V_{DD} ,C_L = 30pF	SM5009AN1S, CF5009AN1 SM5009AN2S, CF5009AN2	–	5	12	
			SM5009AN3S, CF5009AN3 SM5009AN4S, CF5009AN4 SM5009AN5S, CF5009AN5 SM5009AN6S, CF5009AN6 SM5009CN1S, CF5009CN1 SM5009CN2S, CF5009CN2	–	7	16	
Output fall time	t_{f1}	Measurement cct 3, load cct 2, 0.9V_{DD} to 0.1V_{DD} ,C_L = 15pF	SM5009AN1S, CF5009AN1 SM5009AN2S, CF5009AN2	–	3.5	9	ns
			SM5009AN3S, CF5009AN3 SM5009AN4S, CF5009AN4 SM5009AN5S, CF5009AN5 SM5009AN6S, CF5009AN6 SM5009CN1S, CF5009CN1 SM5009CN2S, CF5009CN2	–	5	13	
	t_{f2}	Measurement cct 3, load cct 2, 0.9V_{DD} to 0.1V_{DD} ,C_L = 30pF	SM5009AN1S, CF5009AN1 SM5009AN2S, CF5009AN2	–	5	12	
			SM5009AN3S, CF5009AN3 SM5009AN4S, CF5009AN4 SM5009AN5S, CF5009AN5 SM5009AN6S, CF5009AN6 SM5009CN1S, CF5009CN1 SM5009CN2S, CF5009CN2	–	7	16	
Output duty cycle[1]	Duty	Measurement cct 3, load cct 2, V_{DD} = 3V, Ta = 25°C	C_L = 30 pF, SM5009AN×S, CF5009AN×	45	–	55	%
			C_L = 15 pF, SM5009CN×S, CF5009CN×	40	–	60	
Output disable delay time	t_{PLZ}	Measurement cct 6, load cct 2, V_{DD} = 3V, Ta = 25°C, C_L ≤ 15pF		–	–	100	ns
Output enable delay time	t_{PZL}			–	–	100	ns
Maximum operating frequency	f_{max}	Measurement cct 3	SM5009AN×S, CF5009AN×	40	–	–	MHz
			Ta = −10 to +70°C, SM5009CN×S, CF5009CN×	30	–	–	

1. The duty cycle characteristic is checked the sample chips of each production lot.

5V operation: V_{DD} = 4.5 to 5.5V, V_{SS} = 0V, Ta = –40 to 85°C unless otherwise noted.

Parameter	Symbol	Condition		Rating min	Rating typ	Rating max	Unit
Output rise time	t_{r1}	Measurement cct 3, load cct 2, $0.1V_{DD}$ to $0.9V_{DD}$	C_L = 15pF	–	2	4	ns
	t_{r2}		C_L = 30pF	–	3.5	7	
	t_{r3}		C_L = 50pF	–	4	8	
Output fall time	t_{f1}	Measurement cct 3, load cct 2, $0.9V_{DD}$ to $0.1V_{DD}$	C_L = 15pF	–	2	4	ns
	t_{f2}		C_L = 30pF	–	3.5	7	
	t_{f3}		C_L = 50pF	–	4	8	
Output duty cycle[1]	Duty	Measurement cct 3, load cct 2, V_{DD} = 5V, Ta = 25°C, C_L = 50pF		45	–	55	%
Output disable delay time	t_{PLZ}	Measurement cct 6, load cct 2, V_{DD} = 5V, Ta = 25°C, $C_L \leq$ 15pF		–	–	100	ns
Output enable delay time	t_{PZL}			–	–	100	ns
Maximum operating frequency	f_{max}	Measurement cct 3	SM5009AN×S, CF5009AN×	40	–	–	MHz
			SM5009CN×S, CF5009CN×	30	–	–	

1. The duty cycle characteristic is checked the sample chips of each production lot.

5009AK× series

V_{DD} = 4.5 to 5.5V, V_{SS} = 0V, Ta = –40 to 85°C unless otherwise noted.

Parameter	Symbol	Condition		Rating min	Rating typ	Rating max	Unit
Output rise time	t_r	Measurement cct 3, load cct 1, 0.4V to 2.4V, C_L = 15pF		–	2	6	ns
Output fall time	t_f	Measurement cct 3, load cct 1, 2.4V to 0.4V, C_L = 15pF		–	2	6	ns
Output duty cycle[1]	Duty	Measurement cct 3, load cct 1, V_{DD} = 5V, Ta = 25°C, C_L = 15pF		45	–	55	%
Output disable delay time	t_{PLZ}	Measurement cct 6, load cct 1, V_{DD} = 5V, Ta = 25°C, $C_L \leq$ 15pF		–	–	100	ns
Output enable delay time	t_{PZL}			–	–	100	ns
Maximum operating frequency	f_{max}	Measurement cct 3	Ta = –20 to +80°C	40	–	–	MHz
			Ta = –40 to +85°C	30	–	–	

1. The duty cycle characteristic is checked the sample chips of each production lot.

5009AH× series

3V operation: V_{DD} = 2.7 to 3.3V, V_{SS} = 0V, Ta = −20 to 80°C unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Output rise time	t_{r1}	Measurement cct 3, load cct 2, $0.1V_{DD}$ to $0.9V_{DD}$, C_L = 15pF	–	6	18	ns
Output fall time	t_{f1}	Measurement cct 3, load cct 2, $0.9V_{DD}$ to $0.1V_{DD}$, C_L = 15pF	–	6	18	ns
Output duty cycle[1]	Duty	Measurement cct 3, load cct 2, V_{DD} = 3V, Ta = 25°C, C_L = 15pF	45	–	55	%
Output disable delay time	t_{PLZ}	Measurement cct 6, load cct 2, V_{DD} = 3V, Ta = 25°C, $C_L \leq$ 15pF	–	–	100	ns
Output enable delay time	t_{PZL}		–	–	100	ns
Maximum operating frequency	f_{max}	Measurement cct 3	16	–	–	MHz

1. The duty cycle characteristic is checked the sample chips of each production lot.

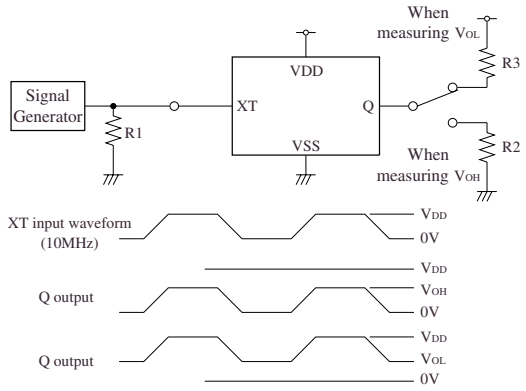
5V operation: V_{DD} = 4.5 to 5.5V, V_{SS} = 0V, Ta = −40 to 85°C unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Output rise time	t_{r1}	Measurement cct 3, load cct 2, $0.1V_{DD}$ to $0.9V_{DD}$, C_L = 15pF	–	4	12	ns
Output fall time	t_{f1}	Measurement cct 3, load cct 2, $0.9V_{DD}$ to $0.1V_{DD}$, C_L = 15pF	–	4	12	ns
Output duty cycle[1]	Duty	Measurement cct 3, load cct 2, V_{DD} = 5V, Ta = 25°C, C_L = 15pF	45	–	55	%
Output disable delay time	t_{PLZ}	Measurement cct 6, load cct 2, V_{DD} = 5V, Ta = 25°C, $C_L \leq$ 15pF	–	–	100	ns
Output enable delay time	t_{PZL}		–	–	100	ns
Maximum operating frequency	f_{max}	Measurement cct 3	30	–	–	MHz

1. The duty cycle characteristic is checked the sample chips of each production lot.

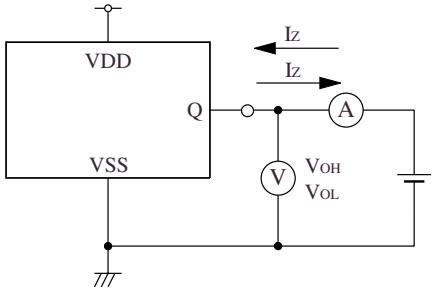
MEASUREMENT CIRCUITS

Measurement cct 1

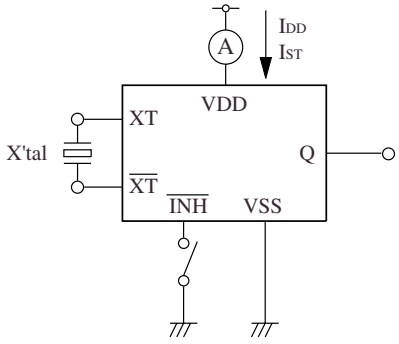


- 5009AK×, AL×, AN1, AN2
  R1: 50Ω
  R2: 250Ω(V_{DD} = 4.5V), 275Ω(V_{DD} = 2.7V)
  R3: 256Ω(V_{DD} = 4.5V), 288Ω(V_{DD} = 2.7V)
- 5009AN3 to AN6, CN×
  R1: 50Ω
  R2: 245Ω(V_{DD} = 4.5V), 262Ω(V_{DD} = 2.7V)
  R3: 256Ω(V_{DD} = 4.5V), 288Ω(V_{DD} = 2.7V)
- 5009AH×
  R1: 50Ω
  R2: 1000Ω(V_{DD} = 4.5V), 1100Ω(V_{DD} = 2.7V)
  R3: 1025Ω(V_{DD} = 4.5V), 1150Ω(V_{DD} = 2.7V)

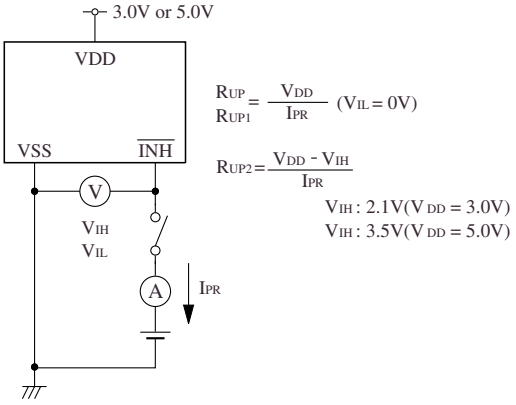
Measurement cct 2



Measurement cct 3



Measurement cct 4

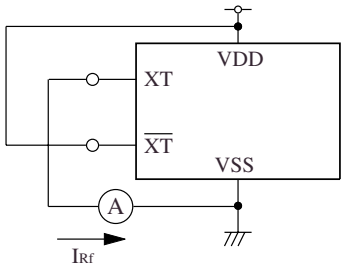


$R_{UP} = R_{UP1} = \frac{V_{DD}}{I_{PR}}$ (V_{IL} = 0V)

$R_{UP2} = \frac{V_{DD} - V_{IH}}{I_{PR}}$

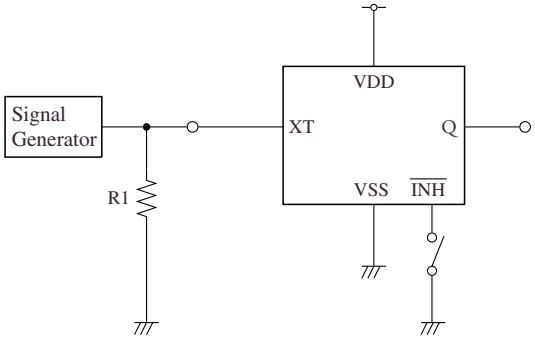
V_{IH} : 2.1V(V_{DD} = 3.0V)
V_{IH} : 3.5V(V_{DD} = 5.0V)

Measurement cct 5



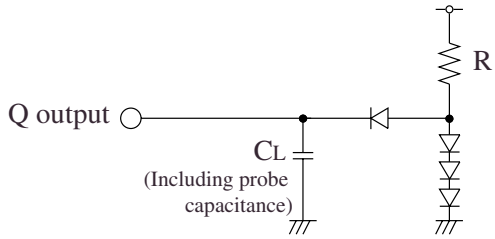
$R_f = \frac{V_{DD}}{I_{Rf}}$

Measurement cct 6



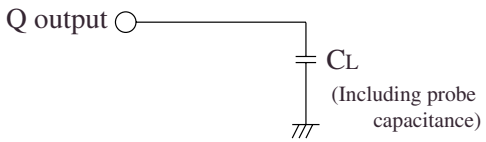
R1: 50Ω

Load cct 1



C_L = 15pF: DUTY, I_{DD}, t_r, t_f
R = 400Ω

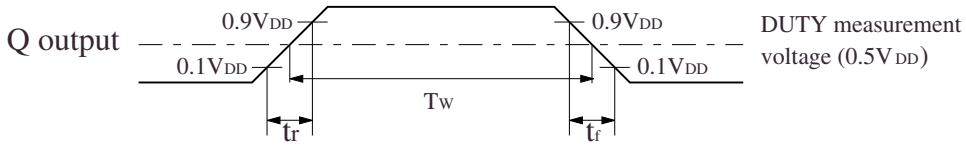
Load cct 2



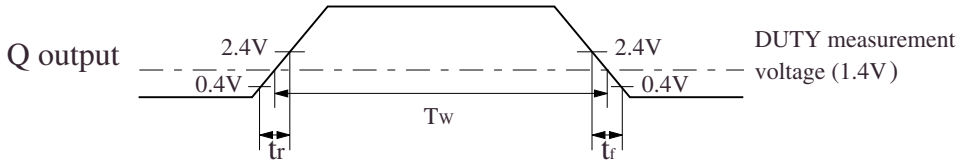
C_L = 15pF: DUTY, I_{DD}, t_{r1}, t_{f1}
C_L = 30pF: t_{r2}, t_{f2}
C_L = 50pF: t_{r3}, t_{f3}

Switching Time Measurement Waveform

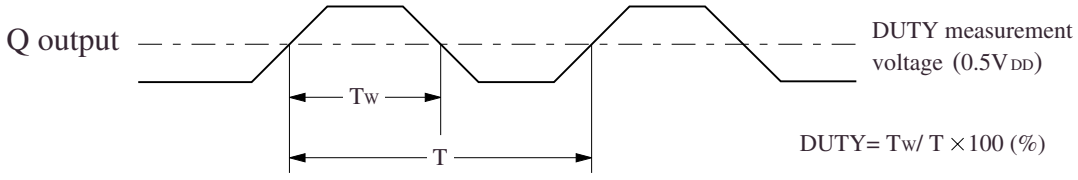
Output duty level (CMOS)



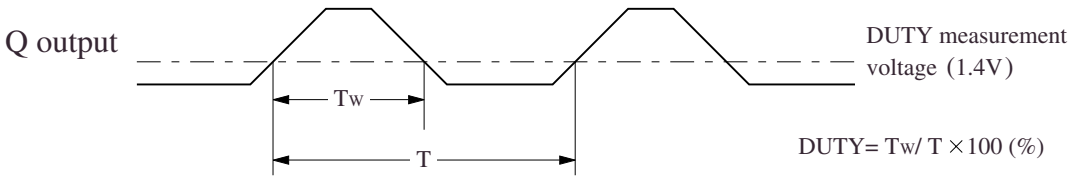
Output duty level (TTL)



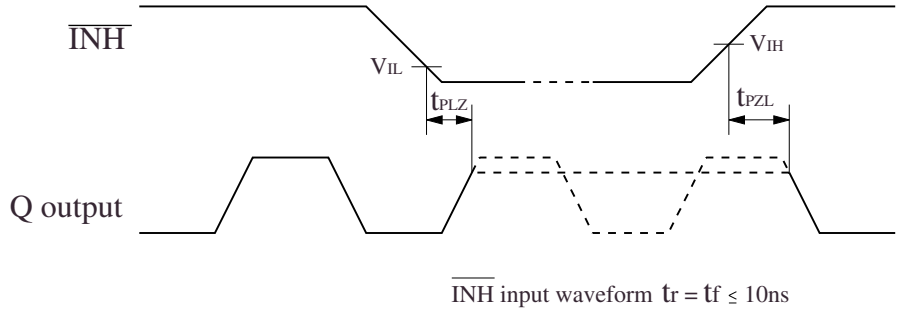
Output duty cycle (CMOS)



Output duty cycle (TTL)



Output Enable/Disable Delay



$\overline{INH}$ input waveform $t_r = t_f \leq 10ns$

Note (AL× series only): when the device is in standby, the oscillator stops. When standby is released, the oscillator starts and stable oscillator output occurs after a short delay.

Please pay your attention to the following points at time of using the products shown in this document.

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